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DILLON & YUDELL LLP
8911 NORTH CAPITAL OF TEXAS HIGHWAY
SUITE 2110
AUSTIN, TX 78759

EXAMINER	
CHOUDHURY, AZIZUL Q	
ART UNIT	**PAPER NUMBER**
2145	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/660,043	BENAYOUN ET AL.	
	Examiner	Art Unit	
	Azizul Choudhury	2145	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-15 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-15 and 17-23* is/are rejected.

7)☒ Claim(s) *24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

This office action is in response to the correspondence received on February 11, 2005.

Claim Objections

Claim 24 is objected to because of the following informalities: The phrase "to the dual-port memory" is followed immediately by the same phrase "to the dual-port memory" in the last line of claim 24 on page 5. This is believed to be a typographical error. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9 and 19 rejected under 35 U.S.C. 102(e) as being anticipated by Narad et al (US Pat No: 6,157,955), hereafter referred to as Narad.

1. With regards to claim 9, Narad teaches a system comprising: a volatile system memory; a non-volatile memory; and a network adapter (Narad teaches a design using PCs with NICs (equivalent to the claimed network adapters) (column 1, lines 57-61,

Narad). Furthermore, it is inherent that PCs contain memory such as those claimed), the network adapter including: a non-system memory capable of temporarily storing a packet received by the network adapter (This is known as a Rx (or receive) buffer (Figure 2, Narad). NICs contain Tx (transfer) buffers and Rx (receive) buffers to aid in controlling the flow of data packets so that it is handled properly); and a microcontroller capable of evaluating the packet received by the network adapter; wherein if the microcontroller determines that the packet is destined for the system's non-volatile memory, then the microcontroller directly transfers the packet from the non-system memory in the network adapter to the system's non-volatile memory, and wherein if the microcontroller does not determine that the packet is destined for the system's non-volatiles memory, then the microcontroller transfers the packet from the non-system memory in the network adapter to the volatile system memory (Narad's design features a Policy Engine (PE) (column 6, line 55 – column 7, line 6, Narad). This policy engine is programmable and is able to implement policies for data packets. This PE is equivalent to the claimed microcontroller and it possesses means by which to route data packets as claimed).

2. With regards to claim 19, Narad teaches a system having a network interface, the network interface comprising: a network interface logic unit composed of: a network connector, and a network controller having a Direct Memory Access (DMA) unit, a system bus interface, a non-system bus interface; a three-port buffer memory having a first port coupled to the network interface logic unit, a second port coupled to

the system bus interface, and a third port coupled to the non-system bus interface, wherein the three-port buffer memory is not memory mapped to a non-volatile memory; and a dedicated microcontroller coupled to the three-port memory, wherein the dedicated microcontroller initializes the DMA unit with a master address that causes an incoming packet of data from a network to be stored locally in the three-port buffer memory, and wherein the non-system bus interface, under the control of the dedicated microcontroller, transfers the packet of data stored in the three-port buffer memory to a non-volatile memory (Narad discloses a network card design. The card features internal memory and busses (Figure 2, Narad). The memory is used for store data packets along with their information and the busses are used to transport the data to a location for processing or to a destination. Plus the card also features DMA (Figures 2 and 12, Narad). The card also features a policy engine (column 6, line 55 – column 7, line 6, Narad). The policy engine is programmable is able to implement policies for data packets. Hence, it has means by which to route data packets. The design also calls for computers and computers commonly use memory such as hard drives. No limitations are placed as to what types of memory are usable and hence all acceptable types (such as dual port memory) are acceptable).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-15, 17-18 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narad in view of Yang et al (US Pat No: 6,526,446), hereafter referred to as Yang.

3. With regards to claim 10, Narad teaches through Yang, a system further comprising: a Small Computer System Interface (SCSI) bus connecting the network adapter to the system's non-volatile memory, wherein a transfer of the packet from the non-system memory in the network adapter to the system's non-volatile memory does not occur via the system bus

(Narad discloses a design for a network interface card with transmit and receive means (Figure 2, Narad) along with busses (Figure 3, Narad). However, the disclosure fails to specifically state the use of SCSI busses.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of

Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

4. With regards to claim 11, Narad teaches through Yang, a system wherein the non-system memory in the network adapter has a first port coupled to a Local Area Network (LAN), a second port coupled to a system bus, and a third port coupled to a SCSI bus

(Networks adapters have non-system memories. At the very least memory must be present to serve as buffers for the transmission and receipt of data. Such memory can be all provided in a single chip within the network card or within a number of chips. Means for such memory are present within Narad's design (Figure 2, Narad). In addition, the claimed LAN, system bus and SCSI bus are all simply pathways for data transmission or receipt. Hence, it is possible for Narad's network card design to have memory attached to the LAN and busses. However, Narad's disclosure fails to specifically state the use of SCSI busses.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of

Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

5. With regards to claim 12, Narad teaches through Yang, a system wherein the system's non-volatile memory is a hard disk in a hard disk drive that has a SCSI interface to the SCSI bus

(Hard disks are widely available in computer systems and the SCSI bus is s common bus used for the hard drive. Narad's design makes use of computers and network cards. However, Narad's disclosure fails to specifically state the use of SCSI busses.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

6. With regards to claim 13, Narad teaches through Yang, a system wherein the microcontroller evaluates the packet by examining in the packet: an address source; an

address destination; and a port number that indicates which transfer protocol is used by the packet, such that only packets having a pre-determined source and address destination and using a pre-determined port are transferred from the non-system memory in the network adapter to the system's non-volatile memory

(Narad's design for a network card processes data packets (column 3, lines 46-49, Narad). It contains a policy engine that reads the data packets and determines how it is to be processed (column 6, line 55 – column 7, line 6, Narad). Plus, the claimed data packet information such as addresses and port and protocol information are available in data packets such as in the header. This information must be read in order to process the data properly. However, Narad's disclosure fails to specifically state the use of SCSI busses.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

7. With regards to claim 14, Narad teaches through Yang, a system wherein the microcontroller locally stores a listing of address sources, address destinations and port numbers that authorize the packet to be routed directly to the system's non-volatile memory

(Narad's design for a network card processes data packets (column 3, lines 46-49, Narad). It contains a policy engine that reads the data packets and determines how it is to be processed (column 6, line 55 – column 7, line 6, Narad). Plus, the claimed data packet information such as addresses and port and protocol information are available in data packets such as in the header. This information must be read in order to process the data properly. Since this data is read, processed and used, it must be stored. If the data is not stored, it cannot be processed. However, Narad's disclosure fails to specifically state the use of SCSI busses.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

8. With regards to claim 15, Narad teaches through Yang, a system wherein the packet is received from a network

(Narad's design for a network card processes data packets (column 3, lines 46-49, Narad). Data packets are transferred through networks. Hence the data packets received must be received from a network. However, Narad's disclosure fails to specifically state the use of SCSI busses.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

9. With regards to claim 17, Narad teaches through Yang, a system for downloading a data file from a web server to a user workstation through a network to which is connected said user workstation, said user workstation including a hard disk for storing a data file being transferred over a Small Computer System Interface (SCSI) bus, said user workstation comprising: a dual port memory for temporarily storing said data file, said dual-port memory having: an input port, a first output port and a second

output port, a network logic unit interconnected between said network and said input port for transmitting said data file to said dual-port memory, a bus interface interconnected between said first output port and a system bus for transmitting a data file from said dual-port memory to a main memory, and a SCSI logic unit interconnected between said second output port and said SCSI bus for transmitting a data file from said dual port memory directly to said hard disk over said SCSI bus, thus bypassing said system bus

(Narad discloses a network card design. The card features internal memory and busses (Figure 2, Narad). The memory is used for store data packets along with their information and the busses are used to transport the data to a location for processing or to a destination. The card also features a policy engine (column 6, line 55 – column 7, line 6, Narad). The policy engine is programmable is able to implement policies for data packets. Hence, it has means by which to route data packets. The design also calls for computers and computers commonly use memory such as hard drives. No limitations are placed as to what types of memory are usable and hence all acceptable types (such as dual port memory) are acceptable. However, Narad's disclosure fails to specifically state the use of SCSI busses.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses

such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

10. With regards to claim 18, Narad teaches through Yang, a system wherein said user workstation comprises a microcontroller for selecting the output port of the dual-port memory used to transmit the data file

(Narad's design makes use of computers and computers all contain microcontrollers. However, Narad's disclosure fails to specifically state the use of SCSI busses.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

11. With regards to claim 20, Narad teaches through Yang, the system wherein the non-system bus interface is a Small Computer System Interface (SCSI) bus interface

(Narad teaches a design for a network card. However the network card design does not disclose the use of a SCSI bus interface.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

12. With regards to claim 21, Narad teaches through Yang, the system wherein the incoming packet of data is never transmitted across a system bus in the system nor is the incoming packet of data ever accessed by a central processor in the system until after the incoming packet of data is stored in the non-volatile memory by the SCSI bus interface

(Narad discloses a design wherein the data packets are processed by the policy engine (column 6, line 55 – column 7, line 6, Narad). The policy engine examines each data packet and determines where the data packet is to be sent and performs such

transmission tasks. However, the network card design does not disclose the use of a SCSI interface.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

13. With regards to claim 22, Narad teaches through Yang the system wherein the microcontroller informs the central processor in the system of the storage and address of the incoming packet of data in the non-volatile memory

(Narad discloses a design wherein the data packets are processed by the policy engine (column 6, line 55 – column 7, line 6, Narad). The policy engine examines each data packet and determines where the data packet is to be sent and performs such transmission tasks. When data is to be sent to a particular location, that location must be aware of the data that is coming towards it. Hence if the data is to be sent to the memory that the central processor monitors, the central processor must be informed as

claimed. However, the network card design does not disclose the use of a SCSI interface.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

14. With regards to claim 23, Narad teaches through Yang the system wherein the central processor subsequently alerts a File Transfer Protocol (FTP) application of the location of the newly stored packet of data

(Narad discloses a design wherein the data packets are processed by the policy engine (column 6, line 55 – column 7, line 6, Narad). The policy engine examines each data packet and determines where the data packet is to be sent and performs such transmission tasks. When data is to be sent to a particular location, that location must be aware of the data that is coming towards it. Hence if the data is to be sent to the memory that the central processor monitors, the central processor must be informed as claimed. If a particular application is needed to fulfill the process request, the central

processor inherently will call upon such an application (such as the claimed ftp application). However, the network card design does not disclose the use of a SCSI interface.

In the same field of endeavor, Yang also teaches a design for a network interface card. The design allows for SCSI interfaces (column 5, lines 58-60, Yang).

Both Narad and Yang disclose designs for network interface cards. While Narad's design fails to disclose the use of SCSI busses, designs such, as Yang's exist which do make use of SCSI busses. In addition, Narad's design does use other busses such as PCI busses (Figure 3, Narad). Therefore, it would have been obvious to one skilled in the art, during the time of the invention, to have combined the teachings of Nard with those of Yang, for the purpose of providing significantly improved data throughput of a network connection (column 2, lines 21-22, Yang)).

Allowable Subject Matter

Claim 24 has allowable subject matter. After amendments satisfying the claim objection are received, claim 24 is allowable.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Remarks

After careful evaluation of the amendment, claim 24 is now viewed as having allowable subject matter. There remains a minor objection with claim 24 but that is believed to be a typographical error. As for the claims 9-15 and 17-23, as they stand unchanged, the prior rejections still stand. It is therefore encouraged that the allowable subject matter of claim 24 be incorporated into the other independent claims in an effort to allow the case.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Azizul Choudhury whose telephone number is (571) 272-3909. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Valencia Martin-Wallace can be reached on (571) 272-6159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AC

V. Martin Wallace

VALENCIA MARTIN-WALLACE
SUPERVISORY PATENT EXAMINER